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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,511	12/05/2001	Francis Edward Noel JR.	RAL920000108US1	8028

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EXAMINER	
AHMED, SALMAN	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,511	NOEL ET AL.	
	Examiner	Art Unit	
	Salman Ahmed	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/13/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/5/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are pending

Claims 1-21 are rejected.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 6, 9, 10, 13, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassing (C6x solutions for voice over IP gateway, Northcon/98 Conference Proceedings 21-23 Oct. 1998 Page(s):74 – 85) in view of Chou et al. (System-on-a-chip design for modern communications: Circuits and Devices Magazine,

IEEE Pub Date Nov 2001, Volume 17, Issue 6, On pages 12-17), hereinafter referred to as Chou.

In regards to claim 6, Cassing teaches a network processor integrated circuit (IC) (figure 4) comprising: an embedded processor complex (EPC) with multiple processors (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner) implement in the IC; a first communication interface from the IC to physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet), a second interface from the IC to a switch fabric (figure 4, T8100 Time Slot Interchange (TSI) switch); a memory storage unit (figure 4, SDRAM) implemented in the IC; a digital signal processor (DSP) (figure 4, TMS32OC6201 DSPs) implemented in the IC having an analog I/0 (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) and a digital I/0 interface (page 77 table 1, Serial port forms a glue-less interface to TDM frames); and a bus system for coupling said EPC, said physical layer devices, said switch fabric, said storage unit and said DSP (figure 4, shaded bus connection connecting various modules and page 74, section: *Gateway Architectural Requirements* Fast Arbitrated Bus: A high-speed bus for communications among modules).

In regards to claim 13 Cassing teaches a method for improving the performance and functionality of a network processor (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded

processors for hosting networking protocols in fault-tolerant distributed manner) integrated circuit controlling the communication between physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet) comprising the steps of: adding a DSP core (figure 4, TMS32OC6201 DSPs) to network processor (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner) IC; coupling digital signals (page 77 table 1, Serial port forms a glue-less interface to TDM frames) to and from said network processor IC and said DSP core; executing instructions by said DSP to determine a characteristic of said digital signals (page 76, last paragraph, the DSP subsystem is the most computationally intensive part of the voice gateways. The DSP subsystem hosts the following functions. Group 3 Fax Modems, Echo Cancellers, Voice encoder and decoders such as ITU-T standard speech coders Telephony signaling tone generators and detectors and HDLC processing for LAPD signaling); and directing a dispensation of digital signals based on said determined characteristic (page 77, last paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets. The i960 IOP, performs the function of routing the packets to the PCI bus. The IOP acts as a host for networking protocols. The IOP can also access the TDM signals via the HDLC controller. The HDLC controller allows access to HDLC formatted frames from WAN traffic).

In regards to claims 6 and 13, Cassing does not explicitly teach DSP core and network processors can be implemented in an integrated circuit (IC) environment.

Chou, in the same field of endeavor teaches (page 12, first column) the data communications integrated circuit (IC) industry has grown from emphasis on layer-1 and layer-2 implementations to layer-3 design for modern communication systems. Many basic system functions have been realized on monolithic silicon chips. The overall industrial thrusts are heading toward a 7-layer-architecture-on-a-chip direction. Thus, more sophisticated functional modules will be included on the silicon chips in the foreseeable future. Embedded memory, network processors, mixed-signal front-end, and on-chip caches are selective examples among them. The previous board-level components are becoming modules of an integrated communication IC.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing's system by incorporating the concept of DSP core and network processors being be implemented in a integrated circuit (IC) environment. The motivation is that implementing SOC (System on a chip) is very cost efficient to manufacture, implement and deploy; thus economically benefiting communication equipment manufacturers.

In regards to claim 9, Cassing teaches DSP (figure 4, TMS32OC6201 DSPs) is a functional core external (see figure 4) to EPC (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner), DSP coupled to EPC and to one of physical layer devices (figure 4, J5 physical interface and

page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet).

In regards to claims 10 and 19 Cassing teaches DSP has an analog signal interface (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) for receiving and sending analog signals and a digital signal interface (page 77 table 1, Serial port forms a glue-less interface to TDM frames) for sending and receiving digital signals.

In regards to claim 14, Cassing teaches coupling analog signals (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) to DSP core; digitizing analog signals (page 77 second paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets); processing digitized analog signals by DSP (page 77 second paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets) core; incorporating processed digital signals into data packets corresponding to a communication protocol (page 79, 1st paragraph, Efficient canned support for TDM buffering, packetized speech. Low delay jitter buffer for pacektized speech), and receiving and transmitting data packets of processed digital signals to physical layer devices on a communication network coupled to network processor (page 77, last paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets. The i960 IOP, performs the function of routing the packets to the PCI bus. The IOP acts as a host for networking protocols. The IOP can also access the TDM signals via the HDLC

controller. The HDLC controller allows access to HDLC formatted frames from WAN traffic) IC.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravindranath et al. (US PAT 6987756), hereinafter referred to as Ravindranath in view of Wolf et al. (Design Issues for High-Performance Active Routers, Selected Areas in Communications, IEEE Journal on Volume 19, Issue 3, March 2001 Page(s):404 – 409) and further in view of Chou.

In regards to claim 1, Ravindranath teaches circuit for data communication comprising: a digital signal processor (figure 3a, the DSP/CODEC 315); circuitry (figure 3a, a telephone interface 310) for receiving digital signals from physical layer devices within a communication network (column 8 lines 64-66, If the endpoint is a digital telephone or equivalent, the telephone interface 310 is a digital telephone interface); circuitry (figure 3a, a telephone interface 310) for receiving analog signals from a selected one of said physical layer devices (column 8 lines 61-63, If the endpoint is an analog telephone or equivalent, the telephone interface 310 is an analog telephone interface), circuitry (figure 3a, processor 345) for routing (column 9 lines 38-41, the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315, the protocol of the media, etc.) analog and digital signals to digital signal processor (DSP) (figure 3a, the DSP/CODEC 315), the DSP outputting processed signals (column 9 lines 1-7, the DSP/CODEC 315 converts analog signals into a digital bit stream on bus 325 (in the case of an analog interface), or converts a digital input into a digital bit

stream on bus 325 (in the case of a digital interface) using one of a number of compression algorithms) in response to DSP programming commands (column 9 lines 38-41, the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315), circuitry (figure 3a, conversion module 330) for incorporating particular processed digital signals into data packets corresponding to a communication protocol (column 9 lines 7-12, the digital bit stream on bus 325 is received by a conversion module 330, which converts the bit stream into packets, cells, etc. depending on the format selected by the terminal gateway 300); and circuitry (figure 3a, network interface module 335) for receiving and transmitting data packets of a communication protocol to and from a network coupling physical layer devices (column 9 lines 14-17, the network interface module 335 includes input/output first-in first-out devices (FIFOs), a transceiver, and timing circuits for transmitting packets, cells, etc. on the network cloud. Packets, cells, etc. received from the network cloud propagate in the opposite direction).

Ravindranath does not explicitly teach the circuit being an integrated circuit (IC).

Wolf in the same field of endeavor teaches multiple network processors with cache and memory on a single application specific integrated circuit are used to overcome the limitations of traditional single processor systems (Abstract).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ravindranath's system by incorporating it in an integrated circuit as taught by Wolf. The motivation is that (as suggested by Wolf, abstract; page 404, first column 2nd paragraph; conclusion) multiple network processors with cache and memory

on a single application specific integrated circuit are used to overcome the limitations of traditional single processor systems. At the same time, continuing advances in integrated circuit technology are making it possible to implement several complete processor subsystems on a single chip. Such method provides a useful basis for extrapolation, as underlying IC technologies continue their inexorable progress to ever-smaller geometries and higher performance levels.

In regards to claim 1, Cassing does not explicitly teach DSP core and network processors can be implemented in a integrated circuit (IC) environment.

Chou, in the same field of endeavor teaches (page 12, first column) the data communications integrated circuit (IC) industry has grown from emphasis on layer-1 and layer-2 implementations to layer-3 design for modern communication systems. Many basic system functions have been realized on monolithic silicon chips. The overall industrial thrusts are heading toward a 7-layer-architecture-on-a-chip direction. Thus, more sophisticated functional modules will be included on the silicon chips in the foreseeable future. Embedded memory, network processors, mixed-signal front-end, and on-chip caches are selective examples among them. The previous board-level components are becoming modules of an integrated communication IC.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing's system by incorporating the concept of DSP core and network processors being be implemented in a integrated circuit (IC) environment. The motivation is that implementing SOC (System on a chip) is very cost efficient to

manufacture, implement and deploy; thus economically benefiting communication equipment manufacturers.

In regards to claim 2, Ravindranath teaches circuitry for outputting analog signals derived from particular ones of processed signals from DSP to a particular one of physical layer devices (column 9 lines 17-21, Packets, cells, etc. received from the network cloud propagates in the opposite direction. In the case of media, the packets, cells, etc. propagate through the conversion module 330, DSP/CODEC 315, telephone interface 310, and to the appropriate endpoint).

In regards to claim 3, Ravindranath teaches DSP receives digital data not derived from a corresponding analog signal (column 8 lines 64-66, If the endpoint is a digital telephone or equivalent, the telephone interface 310 is a digital telephone interface).

In regards to claim 4, Ravindranath teaches selected first digital data from d DSP are analyzed by a network processor to determine a characteristic of first digital data, characteristic used in network processor to direct a dispensation of first digital data (column 9 lines 47-60, the DSP/CODEC 315 and/or telephone interface 310 forward signaling messages or commands received from the endpoint(s) to the endpoint message stack (e.g., off-hook, dialing, pressing transfer key, etc.) for processing by the processor 345. The processor 345 also sends commands to the DSP/CODEC 315 and/or telephone interface 310 for providing call processing functions to the endpoint (e.g., dialtone, ring, ringback, busy, etc.). The network interface module 335 and/or conversion module 330 forward messages received from telephony servers to the

server message stack for processing by the processor 345 (e.g., dialtone message). The processor 345 sends messages to the conversion module 330 and/or the network interface module 335 for transmission to the telephony servers (e.g., off-hook message)).

In regards to claim 5, Ravindranath teaches processing to determine characteristic of first digital data comprises a pattern recognition algorithm (column 9 lines 27-29, the processor 345 detects an off-hook signal from the telephone interface 310).

5. Claims 7, 8, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassing in view of Chou as applied to claims 6 and 13 above and further in view of Chan et al. (US PAT 6826177), hereinafter referred to as Chan.

In regards to 7, 8, 16, 17 and 18 Cassing and Chou teach using DSP core and IC processors for implementing network communication as described in the rejections of claims 6 and 13 above.

Cassing and Chou do not explicitly teach DSP is one of multiple processors in EPC and DSP is a functional core integrated into each one of multiple processors in EPC.

Chan in the same field of endeavor teaches a packet telephony appliance having a network processor that integrates networking and DSP functions (column 1 lines 51-53).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing and Chou's system by incorporating the concept of integration of dsp within processors as taught by Chan. The motivation is that (as suggested by Chan, column 11 lines 46-49) such system is based on the Euphony network processor that integrates networking and DSP functions to provide a low cost and efficient solution for building networked appliances.

In regards to 18 Cassing teaches DSP coupled to one of physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet).

6. Claims 11, 12, 15, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassing in view of Chou as applied to claims 6 and 13 above and further in view of Ravindranath.

Cassing and Chou teach doing message processing using DSP core as described in the rejections of claims 6 and 13 above.

Cassing and Chou do not explicitly teach Dsp receives program commands via switch fabric from a remote device and receives program commands via a general-purpose processor in network processor IC.

Ravindranath in the same field of endeavor teaches the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315, the protocol of the media, etc. (column 9, lines 38-40). Ravindranath in the same field of endeavor further

teaches the DSP/CODEC 315 and/or telephone interface 310 forward signaling messages or commands received from the endpoint(s) to the endpoint message stack (e.g., off-hook, dialing, pressing transfer key, etc.) for processing by the processor 345 (column 9 lines 47-51).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing and Chou's system by incorporating the concept of dsp receiving commands from network and processor as taught by Ravindranath. The motivation is that by having dsp taking some of the processing responsibility from the processor via receiving commands from the network and processor, dsp will leave processors free to do other processing thus making the system robust.

Response to Arguments

7. Applicant's arguments see page 6 of the Remarks section, filed 7/13/2006, with respect to the U.S.C. 112 second paragraph rejection has been fully considered and are persuasive. The U.S.C. 112 second paragraph rejection has been withdrawn.

Applicant's arguments see pages 6-14 of the Remarks section, filed 7/13/2006, with respect to the U.S.C. 102 rejections of claims have been fully considered and are not persuasive.

Applicant argues, see last paragraph of page 7 and 1-2 paragraphs of page 8 of the Remarks section, the rejection of Claim 6 under 35 U.S.C 102(b) as being anticipated by Cassîng is traversed by an article by "Electronicstalk", published August 2005, stating "These issues centre on various ways digital signal processor (DSP)

modem and network processor chips might be integrated in digital subscriber line access multiplexer (DSLAM) equipment. So far these two types of chips -among the industry's most intriguing-have not been combined on the same chip". Applicant further argues that in 1998 4-8 M byte of memory would not be integrated on a single IC.

However, Examiner respectfully disagrees with this traversal; as Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. As such, further response to the arguments on this issue is moot. Examiner takes note of the article by "Electronicstalk", published August 2005 cited by the Applicant.

Examiner respectfully disagrees with the Applicant's traversal (see page 8 paragraph 3) of claims 9-10 for the same reasons mention above.

In regards to claims 13, 14 and 19 Applicant argues, see paragraphs 4-5 of page 8 of the Remarks section, Cassing does not anticipate a network processor IC with an integrated DSP functionality and thus does not anticipate a method for improving the performance of a network processor IC by adding DSP functionality.

However, Examiner respectfully disagrees with this traversal; as Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. As such, further response to the arguments on this issue is moot.

In regards to claim 1, see page 9 and paragraphs 1-2 of page 10 of the Remarks section, the Applicant asserts that the rejection of Claim 1 under JJ U.S.C. 103(a) as being unpatentable over Ravindranath in view of Wolf traversed by an article by "Electronicstalk", published August 2005 and by the argument there is no teaching or

suggestion in Ravindranath to combine the functionality of a network processor with a DSP on a single IC.

However, examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language and the amendments to the claims, necessitated the new ground(s) of rejection presented in this Office action. As such, further response to the arguments on this issue is moot. Examiner also respectfully disagrees with the Applicant's argument, (see page 10 paragraphs 3-4 of the remark section) regarding the allowability of the claims 2-5 for the reasons mentioned above.

In regards to claims 7-8 and 16-18, see last paragraphs of page 10 and paragraphs 1-2 of page 11 of the Remarks section, the Applicant argues at the time when Chan reference was filed (June 2001), no one had integrated a network processor and DSP functionality on a single integrated circuit (IC). Applicant asserts that one of ordinary skill in the art could not combine the teachings of Cassing and Chan to arrive at the invention of Claim 6. The Applicant asserts that Cassing and Chan, singly or in combination, do not teach the invention of Claim 7-8 and 16-18. Applicant further argues Claim 7 adds the limitation that one of the processors in the EPC in the single IC is the DSP. The Office Action states that Cassing does not explicitly teach that the DSP is one of the processors in the EPC.

However, examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language and the amendments to the claims, necessitated the new ground(s) of rejection

presented in this Office action. As such, further response to the arguments on this issue is moot. Examiner further points out, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art at the time the invention was made. See In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In regards to claims 11, 12, 15, 20 and 21 see last paragraphs of page 11 and page 12 of the Remarks section, the Applicant argues Ravindranath does not teach or suggest that the DSP receives program commands from a general purpose processor that is on the same chip as the network processor as recited in Claim 12. Therefore, the Applicant asserts that the rejections of Claims 11-12 under .35 US.C. l03(a) as being unpatentable over Cassing in view of Ravindranath are traversed for the above arguments and for the same reasons as Claim 6. Applicant further adds, the Office Action does not specifically address Claims 15 and 20-21 relative to the rejections U.S.C. 103(a) as being unpatentable over Cassing in view of Ravindranath and therefore fails to make a prima facie case of obviousness.

However, Examiner respectfully disagrees with this traversal; as Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. As such, further response to the arguments on this issue is moot. As mentioned earlier, Examiner respectfully points out that, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the

primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art at the time the invention was made. See In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 2616

SA
7/18/2006

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